HP 13255

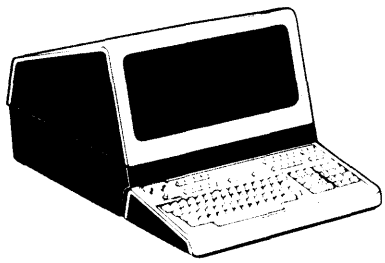
PROCESSOR (8080A-2) MODULE

Manual Part No. 13255-91093

PRINTED

AUG-01-76

DATA TERMINAL
TECHNICAL INFORMATION



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1.0 INTRODUCTION.

The Processor (8080A-2) Module functions as the main controlling unit for the terminal. The processor fetches instructions from memory and performs I/O operations on other modules attached to the terminal data bus (Backplane Assembly). The Processor (8080A-2) Module has the capability of accessing either the standard backplane bus or a special top plane bus defined later.

2.0 OPERATING PARAMETERS.

A summary of operating parameters for the Processor (8080A-2) Module is contained in tables 1.0 through 5.1.

Table 1.0 Physical Parameters

Part Number	Nomenclature	Size (L x W x D) +/-0.100 Inches	Weight (Pounds)
02640-60093	Processor (8080A-2) PCA	12.5 x 4.0 x 0.5	0.63
Number of Backplane Slots Required: 1			

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NOTE: This document is part of the 264XX DATA TERMINAL product series Technical Information Package (HP 13255).

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Number of Backplane Slots Required: 1			

Table 2.0 Reliability and Environmental Information

Environmental: (X) HP Class B ( ) Other:
Restrictions: Type tested at product level
Failure Rate: 1.267 (percent per 1000 hours)

Table 3.0 Power Supply and Clock Requirements - Measured
(At +/-5% Unless Otherwise Specified)

+5 Volt Supply	+12 Volt Supply	-12 Volt Supply	+42 Volt Supply
@ 300 mA	@ 60 mA	@ 2 mA	@ mA
			NOT APPLICABLE

115 volts ac	220 volts ac
@ A	@ A
NOT APPLICABLE	NOT APPLICABLE

Clock Frequency: 4.915 MHz (+0.01% -0.01%)

Table 4.0 Jumper Definitions

PCA Designation	Function	
	In	Out
MSBI	Do Not Invert $\overline{\text{ADDR14}}$ and $\overline{\text{ADDR15}}$	Invert $\overline{\text{ADDR14}}$ and $\overline{\text{ADDR15}}$
CTUI	Enable CTU Interrupts	Disable CTU Interrupts
DCI	Enable Data Comm Interrupts	Disable Data Comm Interrupts
PAE	Enable $\overline{\text{PROC ACTIVE}}$ Driver	Disable $\overline{\text{PROC ACTIVE}}$ Driver
HLTE	Allow RUN/Halt From RUN Line	RUN Always, No Halt
POLL	Allow Assertion of $\overline{\text{POLL}}$	Do Not Allow Assertion of $\overline{\text{POLL}}$

5.0 Connector Information

Connector and Pin No.	Signal Name	Signal Description
P1, Pin 1	+5V	+5 Volt Power Supply
-2	GND	Ground Common Return (Power and Signal)
-3	SYS CLK	4.915 MHz System Clock
-4	-12V	-12 Volt Power Supply
-5	$\overline{\text{ADDR0}}$	Negative True, Address Bit 0
-6	$\overline{\text{ADDR1}}$	Negative True, Address Bit 1
-7	$\overline{\text{ADDR2}}$	Negative True, Address Bit 2
-8	$\overline{\text{ADDR3}}$	Negative True, Address Bit 3
-9	$\overline{\text{ADDR4}}$	Negative True, Address Bit 4
-10	$\overline{\text{ADDR5}}$	Negative True, Address Bit 5
-11	$\overline{\text{ADDR6}}$	Negative True, Address Bit 6
-12	$\overline{\text{ADDR7}}$	Negative True, Address Bit 7
-13	$\overline{\text{ADDR8}}$	Negative True, Address Bit 8
-14	$\overline{\text{ADDR9}}$	Negative True, Address Bit 9
-15	$\overline{\text{ADDR10}}$	Negative True, Address Bit 10
-16	$\overline{\text{ADDR11}}$	Negative True, Address Bit 11
-17	$\overline{\text{ADDR12}}$	Negative True, Address Bit 12
-18	$\overline{\text{ADDR13}}$	Negative True, Address Bit 13
-19	$\overline{\text{ADDR14}}$	Negative True, Address Bit 14
-20	$\overline{\text{ADDR15}}$	Negative True, Address Bit 15
-21	$\overline{\text{I/O}}$	Negative True, Input Output/Memory
-22	GND	Ground Common Return (Power and Signal)

Table 5.0 Connector Information (Cont'd.)

Connector and Pin No.	Signal Name	Signal Description
P1, Pin A	GND	Ground Common Return (Power and Signal)
-B	$\overline{\text{POLL}}$	Negative True, Polled Interrupt Identification Request
-C	+12V	+12 Volt Power Supply
-D	PWR ON	System Power On
-E	$\overline{\text{BUS0}}$	Negative True, Data Bus Bit 0
-F	$\overline{\text{BUS1}}$	Negative True, Data Bus Bit 1
-H	$\overline{\text{BUS2}}$	Negative True, Data Bus Bit 2
-J	$\overline{\text{BUS3}}$	Negative True, Data Bus Bit 3
-K	$\overline{\text{BUS4}}$	Negative True, Data Bus Bit 4
-L	$\overline{\text{BUS5}}$	Negative True, Data Bus Bit 5
-M	$\overline{\text{BUS6}}$	Negative True, Data Bus Bit 6
-N	$\overline{\text{BUS7}}$	Negative True, Data Bus Bit 7
-P	$\overline{\text{WRITE}}$	Negative True, Write/Read Type Cycle
-R	$\overline{\text{ATN2}}$	Negative True, CTU and Polled Interrupt Request
-S	$\overline{\text{WAIT}}$	Negative True, Wait Control Line
-T	PRIOR IN	Bus Controller Priority In
-U	PRIOR OUT	Bus Controller Priority Out
-V	PROC ACTIVE	Negative True, Processor Active (Controlling Bus)
-W	$\overline{\text{BUSY}}$	Negative True, Bus Currently Busy (Not Available)
-X	RUN	Allow Processor to Access Bus
-Y	$\overline{\text{REQ}}$	Negative True, Request (Bus Data Currently Valid)
-Z	$\overline{\text{ATN}}$	Negative True, Data Comm Interrupt Request

Table 5.1 Connector Information

Connector and Pin No.	Signal Name	Signal Description
P3, Pin 1	GND	Ground
- 2	ADDR0	Address Bit 0
- 3	ADDR1	Address Bit 1
- 4	ADDR2	Address Bit 2
- 5	ADDR3	Address Bit 3
- 6	ADDR4	Address Bit 4
- 7	ADDR5	Address Bit 5
- 8	ADDR6	Address Bit 6
- 9	ADDR7	Address Bit 7
-10	ADDR8	Address Bit 8
-11	ADDR9	Address Bit 9
-12	ADDR10	Address Bit 10
-13	ADDR11	Address Bit 11
-14	ADDR12	Address Bit 12
-15	ADDR13	Address Bit 13
-16	ADDR14	Address Bit 14
-17	ADDR15	Address Bit 15
-18	$\overline{\text{TOP ACTIVE}}$	Negative True, (Low) Indicates Top Plane Module Address Recognition. (High Causes a Bottom Plane Bus Cycle)
-19	READ	High Indicates Top Plane Bus Data Should Be Gated On
-20	WRITE	High Indicates Top Plane Bus Data is Valid
-21	SYNC.PHASE1	Positive Pulse of 100 nSec at Beginning of Processor Major Cycle
-22	GND	Ground

Table 5.1 Connector Information (Cont'd.)

Connector and Pin No.	Signal Name	Signal Description
P3, Pin A	GND	Ground
-B	DBIT0	Data Bit 0
-C	DBIT1	Data Bit 1
-D	DBIT2	Data Bit 2
-E	DBIT3	Data Bit 3
-F	DBIT4	Data Bit 4
-H	DBIT5	Data Bit 5
-J	DBIT6	Data Bit 6
-K	DBIT7	Data Bit 7
-L	$\overline{\text{INT60}}$	Negative True, (Low) Causes Processor Interrupt Request to Address 60 (octal)
-M	$\overline{\text{INT20}}$	Negative True, (Low) Causes Processor Interrupt Request to Address 20 (octal) (Maskable by Firmware)
-N	$\overline{\text{TOP WAIT}}$	Negative True, (Low) Causes Processor Wait States to Synchronize Processor With Slow Memories
-P	$\overline{\text{I/O}}$	Negative True, (Low) Indicates (A15 A14 A13 A12) = (1000)

Table 5.1 Connector Information (Cont'd.)

Connector and Pin No.	Signal Name	Signal Description
-R	SYNC	High Indicates Processor Status is Valid on Top Plane Data Bus
-S	HLTA	High Indicates Processor is Halted
-T	WO	High Indicates Write or Output Cycle
-U	DISABLE ROM	High Indicates Future Read Cycles Should Be Acknowledged by RAM, not ROM
-V	POLL	High Indicates That Devices With Interrupts Pending Should Assert Their ID Code on Data Bus During Next $\overline{I/O}$. READ (Same as Bottom Plane $\overline{POLL}$)
-W	STACK	High Indicates Current Processor Cycle is a Stack Access, Either Read or Write
-X	MEMR	High Indicates Current Cycle is a Memory Read
-Y	$\overline{TOP\ GO\ SLOW}$	Negative True, (Low) Causes Current Processor Clock Cycle to be 500 nSec Instead of Usual 400 nSec Cycle
-Z	GND	Ground

3.0 FUNCTIONAL DESCRIPTION. Refer to the block diagram (figure 1), schematic diagram (figure 2), the timing diagrams (figures 3, 4, and 5), the component location diagram (figure 6), and the parts list (02640-60093) located in the appendix.

The Processor (8080A-2) PCA is the main controller in the terminal. It consists of a clock generator, bus controller, data driver/receiver latch, priority interrupt, address drivers, ready latch, and status/mode latch functional blocks.

3.1 CLOCK GENERATOR.

3.1.1 The clock generator runs from the 4.915 MHz bus System Clock which is first doubled, then divided by either 4 or 5 (U211) to produce the 2-phase non-overlapping clock required by the 8080A-2. The clock generator divides by 4 to give a 400-nanosecond clock cycle, and by 5 to give a 500-nanosecond cycle. The decision to generate a long cycle is made at the beginning of PHASE2 by monitoring the $\overline{\text{TOP GO SLOW}}$ signal (P3, Pin Y). Top plane memories or devices with long access time may pull this line low when an access time of more than 400 but less than 500 nanoseconds is needed. If a module wants more than 500 nanoseconds it must resort to use of the $\overline{\text{TOP WAIT}}$ line, which will cause access time to be stretched out by increments of 400 nanoseconds until the line is released.

The clock generator will generate only 500 nanosecond cycles if test point 4 (labeled SLOW) is grounded. This is a convenience when the INTEL ICE-80 test chip is to be used with the processor since the ICE-80 is specified at 500 nanoseconds minimum clock period.

3.1.2 The bus System Clock (4.915 MHz) on P1, Pin 3 is buffered by U38, Pin 6 and goes to the clock doubler (U111, Pins 11, 12, and 13) and (U411, Pins 3, 4, 5, and 6). U411, Pin 4 drives discrete delay line L1-C6 which is buffered by U411, Pins 5 and 6. U411, Pin 6 drives exclusive OR U111, Pin 13 which compares the clock with the delayed (by 50 nanoseconds) clock to produce a 50 nanosecond pulse for every clock edge, either positive going or negative going.

This doubled clock drives the clock divider U211, Pin 2 which is connected as a synchronous divider selectable between divide-by-4 and divide-by-5. The counter cycles up to state 9, then CARRY (U211, Pin 15) enables a synchronous load (U211, Pin 9) on the next clock. The

parallel data inputs are set to either 5 or 6 depending upon the long/ short select signal at U511, Pin 3. This in turn is the negative OR of either test point SLOW (TP4) or SYNC and $\overline{\text{TOP GO SLOW}}$ (generated by U49, Pins 12 and 13).

The CARRY output U211, Pin 15 during state 9 is the TTL PHASE1 clock, and the complemented QD during all states expect 8 or 9 forms the TTL PHASE2 clock, both of which are stepped up to 12 volts by U31, the 3245 clock driver.

3.2 BUS CONTROLLER.

3.2.1

The bus controller request latch stretches the bus cycle request out of the 8080A-2, and is cleared when the cycle has been initiated. Since the keyboard does not pull $\overline{\text{WAIT}}$ and cannot withstand minimum $\overline{\text{REQ}}$ cycles, the shortest $\overline{\text{REQ}}$ cycle generated by the processor board is 400 nanoseconds giving a minimum bus cycle of 800 nanoseconds.

The RUN and $\overline{\text{PROC ACTIVE}}$ signals can be disabled by jumpers to allow multiple processors on the same bus, where only one can be the main system processor.

3.2.2

Memory or I/O accesses are ANDed with PHASE1 and $\overline{\text{TOP ACTIVE}}$ to request a backplane bus cycle. This request is latched by U49, Pins 4, 5, and 6 and U59, Pins 1, 2, and 8 through 13. The latch is cleared by PWR ON (U34, Pin 11) or Bus Request Acknowledge (U59, Pin 9 from U410, Pin 9). If RUN is enabled either by being high on P1, Pin X or if W1 is open, then the latch output is allowed to set U510, Pin 6 at the next negative bus clock edge. This pulls down on PRIOR OUT (U511, Pin 11 and P1, Pin U). As soon as PRIOR IN goes high, at the next clock U510, Pin 8 is set. This pulls $\overline{\text{BUSY}}$ on P1, Pin W and pulls on $\overline{\text{PROC ACTIVE}}$ (P1, Pin V) if W2 is installed. In addition, address is driven onto the bus and data if it is a write cycle. One clock later $\overline{\text{REQ}}$ is pulled low when U410, Pin 8 sets. This state is held as long as $\overline{\text{WAIT}}$ is held low. The input request latch has now been cleared (U59, Pin 12). When $\overline{\text{WAIT}}$ goes high U510, Pin 8 will go off at the next clock, ending request and latching read data (U49, Pin 11) to U11, Pin 11. One clock later the address and data are removed from the bus, $\overline{\text{PROC ACTIVE}}$ goes high, and the cycle has been completed.

3.3 DATA DRIVER/RECEIVER LATCH.

3.3.1 The bottom bus data is latched at the end of $\overline{\text{REQ}}$ to hold it until the 8080A-2 is ready for it. This allows holding the bottom bus the minimum time and also provides the 200 nanoseconds address hold time required by the bottom bus protocol. All bottom plane outputs are driven by 74LS38's (U12, U23, U45, U46, U58, U61, and U62).

3.3.2 The top plane address and data lines are driven by 3-state drivers (U32, U33, U44, and U51) which are capable of driving 10 regular TTL loads (16 mA). The top plane control lines (and the most significant four address bits) are low power Schottky totem pole drivers. The latter are sufficient to drive two LS loads per board (assuming a maximum of eight top plane boards connected to a single processor).

3.3.3 The backplane bus read data is latched at the end of $\overline{\text{REQ}}$ by U49, Pin 11 which generates a $\overline{\text{REQ}}$ signal in parallel with that put onto the bus by U58, Pin 11. This insures that the data has been latched up before the responding module can remove the data from the bus. During DBIN of a bottom bus read or input operation, the U11 data is driven onto the 8080A-2 data bus by U22 and U24. This also accomplishes the inversion required between the negative logic backplane bus and the positive logic 8080A-2 data bus.

3.3.4 Since the standard 8080A-2 has an input voltage threshold of about 3.3 volts, the standard TTL high output voltage of about 3 volts does not provide any noise immunity. Therefore, all 8080A-2 pins which are used as driven inputs have been provided with pullup resistors (4.7K) to insure that the signals rise to a full 5.0 volts, thus providing about 1.5 volts of noise immunity. (The data I/O pins of the 8080A-2 have internal pullups.) The driving gate is in some cases a TTL totem pole and the active pullup functions to rapidly drive the signal up to 3 volts, and the pullup resistor then pulls the signal more slowly up to 5 volts.

3.4 PRIORITY INTERRUPT.

3.4.1 The 8080A-2 supports hardware vectored priority interrupt on seven levels. This has been allocated as follows:

PRIORITY	INTERRUPT ADDR	SOURCE	CAN FIRMWARE DISABLE?
Lowest	10	Firmware	No
	20	Top Plane	Yes
	30	10 mSec Timer	Yes
	40	Data Comm PCA's	Yes
	50	CTU I/F PCA	No
	60	Top Plane	No
Highest	70	Test Point	No

Jumpers on the Processor (8080A-2) Module can be set to disable the data comm and CTU interrupts for multiprocessor applications. The $\overline{\text{INT20}}$, timer, and data comm interrupts may be firmware disabled by an output instruction. The disables provide a method of masking undesired interrupts so that interrupts may be re-enabled during processing of interrupts of intermediate priority. Lower priority interrupts are masked off at entry to the interrupt processing routine, then interrupts are enabled, thus providing that higher priority (i.e., unmasked) interrupts may be acknowledged. Subsequent interrupts from the device currently being processed may be considered either higher or lower than the interrupt currently being processed, according to whether it itself is masked.

The $\overline{\text{POLL}}$ line can be driven by firmware and indicates to pollable interrupting devices with pending interrupts that they should identify themselves during the next bus input operation. They do this by ANDing $\overline{\text{POLL}}$, $\overline{\text{I/O}}$, $\overline{\text{REQ}}$, and $\overline{\text{WRITE}}$ and use this signal to pull one bus data line low.

3.4.2 Interrupt requests are passed through the priority request holding latches (U310 and U311) to the priority encoder (U39) and then through U27, Pins 6, 3, and 8 drivers onto the 8080A-2 data bus bits 3, 4, and 5. The purpose of the request latches is to insure that the priority encoder output is stable during the INTA cycle when the request is interpreted as an address. The INTA (U25, Pin 2) signal disables the latch inputs, thus holding whatever requests were pending just previous to INTA. Whatever interrupts are pending at INTA time, the priority encoder puts out the code for the highest priority pending request, which is then gated by DBIN onto the 8080A-2 data bus.

3.4.3 Three of the interrupt sources may be disabled (masked) by a firmware output instruction. Data bits 3, 4, and 5 mask certain interrupts as shown in the output instruction bit coding table. The disable signals from the output data mode latch U26 go to U210 to prevent the interrupt requests from reaching the request latches U311, U310.

3.4.4 U110, U19, and U18 form a divide-by-49152 circuit which divides the 4.9152 MHz SYS CLK down to 100 Hz (10 millisecond period).

At PWR ON, U26, Pin 2 will be set low holding the timer reset by driving U110, Pin 4 and 10 and then through U28, Pin 3 and 4 to U18, Pin 2 and 12 and U19, Pin 2 and 12.

When U26, Pin 2 is set high the timer begins counting CLK pulses. After 10 milliseconds have gone by U18, Pin 10 will go low, U28, Pin 6 will go high and U29, Pin 6 will set (go low) if U26, Pin 5 has been set high. The signal goes through interrupt disable gate U210, Pin 5 to U311, Pin 7 thus entering an interrupt request to the processor.

After the interrupt is acknowledged it is necessary to set U26, Pin 5 low and then high to enable U29, Pin 6 to respond to the next period.

If a precise single interval is desired, U26, Pin 2 must be driven low and then high. The interrupt will occur 10 milliseconds after U26, Pin 2 goes high.

3.5 ADDRESS DRIVERS.

3.5.1 To provide strobes required by existing modules, I/O is mapped out of memory address space. Memory references between 32K and 36K (A15 through A12 = 1000) are interpreted by the hardware as I/O operations and cause the $\overline{I/O}$ bus line to be pulled during the bus cycle. For

firmware writing simplicity, address bits 8 and 4 are interchanged during an I/O operation. This results in module address being mapped as follows:

FIRMWARE ADDRESS	I/O MODULE SELECT BIT	P1 REFERENCE DESIGNATOR
A11	M2	$\overline{\text{ADDR11}}$
A10	M1	$\overline{\text{ADDR10}}$
A9	M0	$\overline{\text{ADDR9}}$
A8	M3	$\overline{\text{ADDR4}}$
A4	STROBE	$\overline{\text{ADDR8}}$

3.5.2 I/O input involves a memory read with a logical address of

A15	A14	A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
1	0	0	0	M2	M1	M0	M3	X	X	X	X	X	X	X	X

where M is module address and X is strobe pattern. I/O output involves a memory write analogous to the read. The 8080A-2 Input instruction is never used and the 8080A-2 Output instruction is used to set processor conditions. The 8080A-2 OUT <X> instruction puts the contents of the accumulator into the mode latch. These bits are interpreted as follows:

MODE BIT	MEANING
0	1 = Timer running
1	0 = Timer interrupt acknowledged 1 = Timer re-enable
2	1 = Firmware interrupt request
3	1 = $\overline{\text{INT20}}$ interrupt held off
4	1 = Data comm interrupt held off
5	1 = Timer interrupt held off
6	1 = Poll interrupts (read with next input operation)
7	1 = Disable top plane ROM

3.5.3 The portion of memory space between 32K and 36K (decimal) is defined as I/O space. Memory operations referencing addresses within this range are translated into I/O operations by the hardware. The detection is done by U36, Pins 8, 9, and 10, U28, Pins 12 and 13, and U48, Pins 1, 2, 12, and 13. This signal (U48, Pin 12) is high for addresses falling within the I/O space and is used to drive the $\overline{I/O}$ line on both the backplane and the top plane.

Additionally, the $\overline{I/O}$ signal causes exchanging of address bits $\overline{ADDR4}$ and $\overline{ADDR8}$ on the backplane only (no exchange on the top plane). This exchange is done by U41, controlled by U48, Pin 12 and is done to make firmware source code easier to read. This has the effect of putting I/O module addresses into logical address bits A11 A10 A9 A8.

3.5.4 Address Bit Invert. To maintain firmware compatibility with the 02640-60009 DMA PCA through the 8080A-2, the two most significant address bits (A15 and A14) may be inverted (if W6 is removed). This allows the top word of display memory to be addressed as though it were at 16K (which is the location where the 02640-60009 DMA PCA expects to find the first link of the display). This results in the following mapping:

LOGICAL MEMORY (PROGRAM ADDR)	PHYSICAL MEMORY (JUMPER ADDR)
0-16K	48K-64K
16K-32K	32K-48K
32K-36K (I/O)	16K-20K
36K-48K	20K-32K
48K-64K (DISPLAY)	0-16K

W6 controls whether A15 and A14 are inverted. The actual inversion is done by U111, Pins 1, 2, and 3, and U111, Pins 10, 9, and 8 if W6 is out. If W6 is installed, then no inversion takes place. This assumes that the 16-bit DMA PCA (02640-60124) is installed. Note that the inverted bits are also sent to the top plane.

3.6 READY LATCH.

3.6.1 The READY signal is sampled at the beginning of PHASE2 to provide a suitable set-up interval. When a bus cycle is requested READY goes low at PHASE1 rise, and when the waiting condition is over, READY will go high at the next rise of PHASE2. With a minimum bottom bus cycle of 800 nanoseconds this will cause two 8080A-2 wait states (1 microsecond). Top plane cycles may result in 0, 1, or more wait states. Top plane accesses which cause 0 Wait states require memory access times of approximately 500 nanoseconds or less.

3.6.2 The ready latch U29, Pin 9 is used to hold off the 8080A-2 while slow responding devices catch up. The latch is set during PHASE1 either if the cycle is a bottom bus cycle (U48, Pins 10 and 11) or a slow top plane bus cycle (U48, Pin 9). Once the latch has been set, the $\overline{\text{TOP}}$ $\overline{\text{WAIT}}$ signal must go away during a PHASE2 so that the latch can clear, since it is sampled continuously while the 8080A-2 is in a Wait state (U43, Pin 24). The latch is cleared at the beginning of PHASE2 of the next cycle after the wait condition is removed. The READY signal is pulled up by 4.7K (R1, Pin 5).

3.7 STATUS/MODE LATCH.

3.7.1 This block consists of two 8-bit latches, status and mode.

3.7.2 U25 holds the 8080A-2 status byte which is sent out during SYNC of each processor execution cycle (multiple clock cycles). These bits identify the type of cycle which is about to be done, whether memory, output, input, stack, interrupt, or halt. This information determines whether a bus cycle will be requested, or whether an opcode (RST) should be jammed, or whether the data output mode latch should be loaded.

3.7.3 U26 is the data output mode latch. It holds 1 byte which is settable from the firmware, to determine various operating modes of the processor board/top plane combination, to disable certain interrupts, to request the firmware interrupt, and to acknowledge timer interrupts.

It is loaded during $\overline{\text{WR}}$ time of an Out instruction. Byte 2 of the Out instruction is not examined and can be considered a don't care condition.

4.0 TOP PLANE BUS.

4.0.1 To allow use of fast memory, provision is made for accessing memory through P3, over a top plane bus. The 8080A-2 puts valid addresses on the top plane at least 120 nanoseconds before the beginning of PHASE1. If no response has been received on $\overline{\text{TOP ACTIVE}}$ (P3, Pin 18) by the beginning of PHASE1, a bottom bus cycle is initiated. Thus top plane memories must recognize their addresses and pull on $\overline{\text{TOP ACTIVE}}$ within 120 nanoseconds to indicate their presence.

The $\overline{\text{TOP WAIT}}$ signal functions analogously to the bottom bus $\overline{\text{WAIT}}$. This control line may be used during refresh of dynamic RAM on the top plane. The $\overline{\text{TOP GO SLOW}}$ signal (P3, Pin Y) provides for slow ROM by allowing an addressed top plane module to ask for a 500-nanosecond processor clock cycle instead of a 400-nanosecond cycle. This means that 100 nanoseconds is added to the processor clock cycle in the cycle following the assertion of SYNC by the 8080A-2. Cycles following the first slow one will be 400-nanosecond cycles. Thus a slow top plane module has the choice of asking for a 100-nanosecond slowdown via $\overline{\text{TOP GO SLOW}}$, or a 400-nanosecond slowdown via $\overline{\text{TOP WAIT}}$.

The top plane bus accessed through P3 of the Processor (8080A-2) PCA is intended as a high speed path to program memory, bypassing the 800-nanosecond minimum wait of the backplane bus.

4.0.2 To minimize the need for jumpers and fixed memory allocations, a handshake method is used allowing the processor to determine without loss of time, whether a given word of memory is accessible over the top plane bus. During processor cycle T1, PHASE1, the processor puts valid addresses onto the top plane. A memory module which recognizes its addresses must pull down the $\overline{\text{TOP ACTIVE}}$ line (P3, Pin 18) within 120 nanoseconds of address recognition. If $\overline{\text{TOP ACTIVE}}$ is still high by T2, PHASE1, the processor assumes the addressed memory is not accessible on the top plane and initiates a request for a backplane bus cycle at the same memory address.

4.0.2.1 Although the primary application of the top plane is program ROM access, it has provisions for I/O and RAM as well. The $\overline{\text{TOP WAIT}}$ line (P3, Pin N) can be used to cause an 8080A-2 wait state (or more than 1) if it is pulled low at the same time the address is recognized. This line is also sampled at T2, PHASE1 and uses the same ready latch as the backplane bus. Thereafter, $\overline{\text{TOP WAIT}}$ is sampled continuously as long as the 8080A-2 is in the Wait state. This permits processor holdoff during a refresh or slow I/O operation. The $\overline{\text{TOP GO SLOW}}$ line can be used by slow memory modules to force a longer than normal clock cycle during access. This gives a 500 nanosecond access time requirement instead of the usual 400 nanoseconds. The timing is the same as for $\overline{\text{TOP ACTIVE}}$.

4.0.2.2 If refreshing is done immediately following memory access during M1 (processor Fetch cycle), no conflict will occur since a minimum of 1 microsecond is available. To enable refresh during Halt the HLTA status bit is available to switch refresh modes (P3, Pin S). For RAM, WO is brought to P3, Pin T indicating that a write is to be done. The WRITE signal on P3, Pin 20 is completely overlapped by address data and WO, and should be used to do the actual writing. The READ line on P3, Pin 19 indicates when data should be gated onto the data bus (P3, Pin B to P3, Pin K). In cases where a ROM loader is to load RAM in the same memory space, a DISABLE ROM line (P3, Pin U) is provided which can be set by firmware. When this line is high it is intended that read operations should be directed at RAM rather than ROM.

There is one more programmable line, POLL on P3, Pin L. Two top plane interrupt lines, $\overline{\text{INT20}}$ (P3, Pin M) and $\overline{\text{INT60}}$ (P3, Pin L) are provided to allow future capability enhancements.

4.0.2.3 The $\overline{\text{I/O}}$ line (P3, Pin P) is the decoded high order address (A15 A14 A13 A12 = 1000) portion of memory space allocated to I/O operations and is provided to simplify decoding of I/O device addresses in the future. The end pins (P3, Pin 1, 22, A, and Pin Z) are grounded on the 8080A-2 Processor PCA. Top plane modules may monitor any of these pins to determine if the top plane is installed. If the top plane is removed, such modules should respond to accesses from the backplane instead. This allows a mode where all transfers take place over the backplane, for diagnostic purposes.

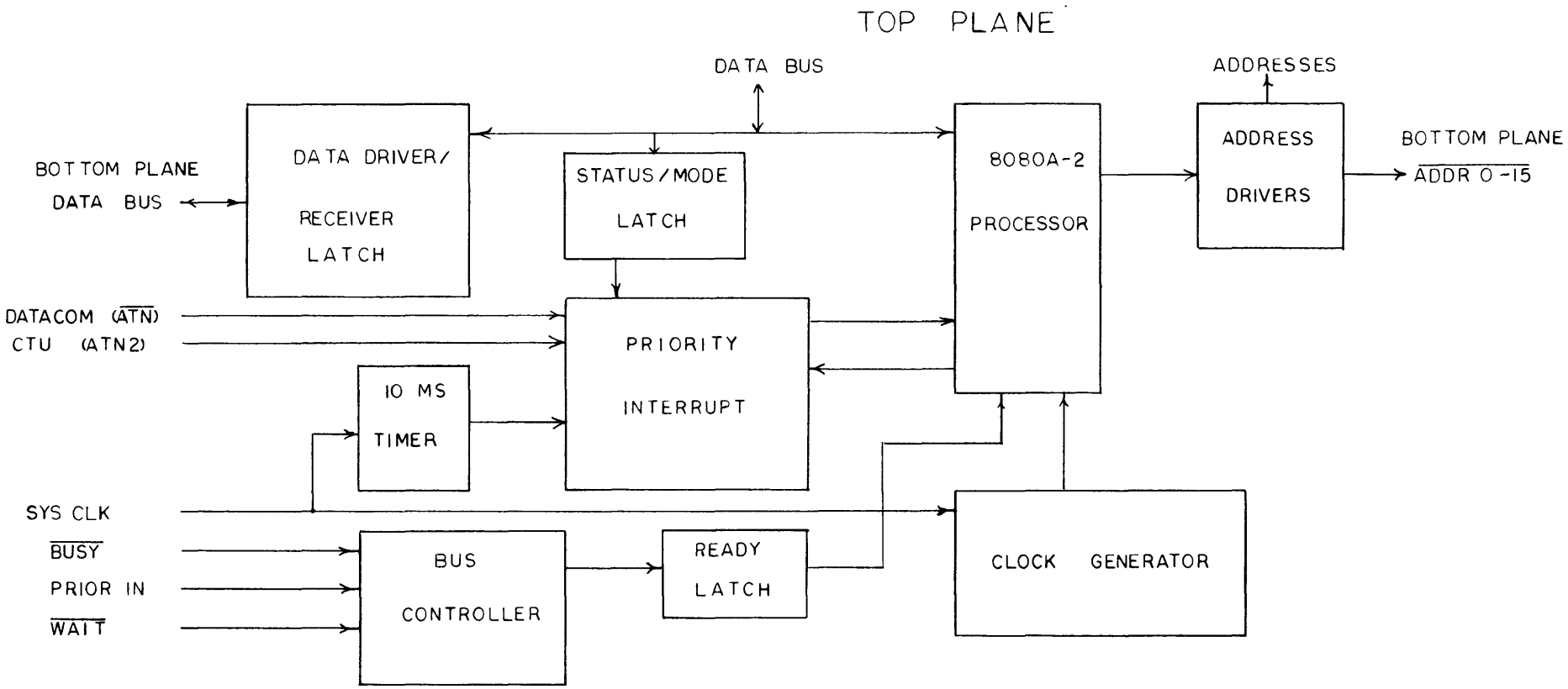

Figure 1
Processor (8080A-2) Block Diagram
AUG-01-76 13255-91093

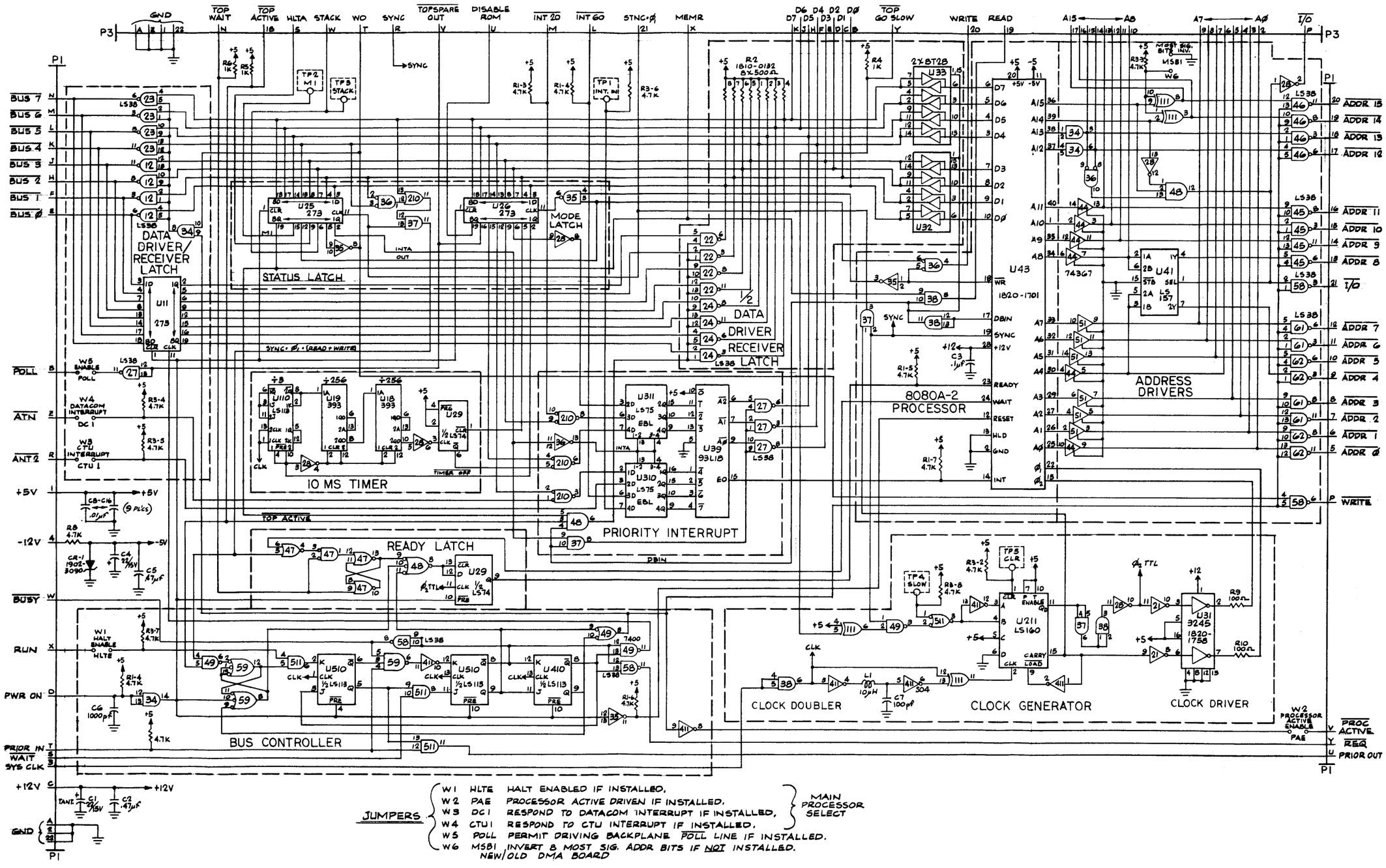

Figure 2
Processor (8080A-2) PCA Schematic Diagram
AUG-01-76 13255-91093

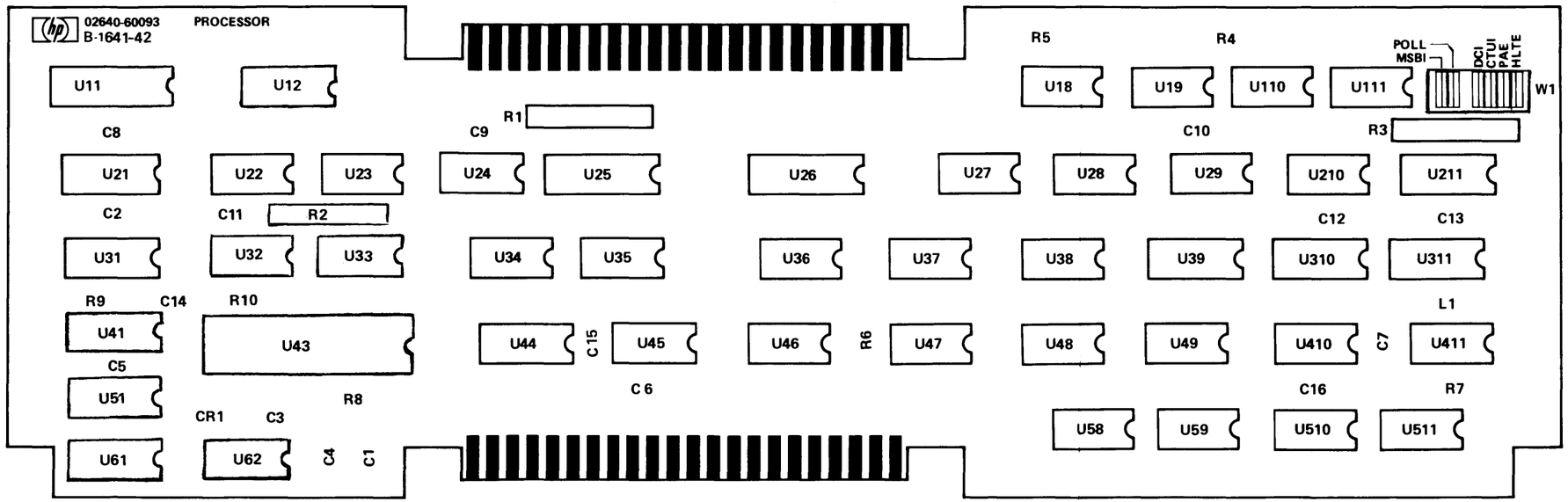

Figure 6
Processor (8080A-2) PCA Component Location Diagram
AUG-01-76 13255-91093

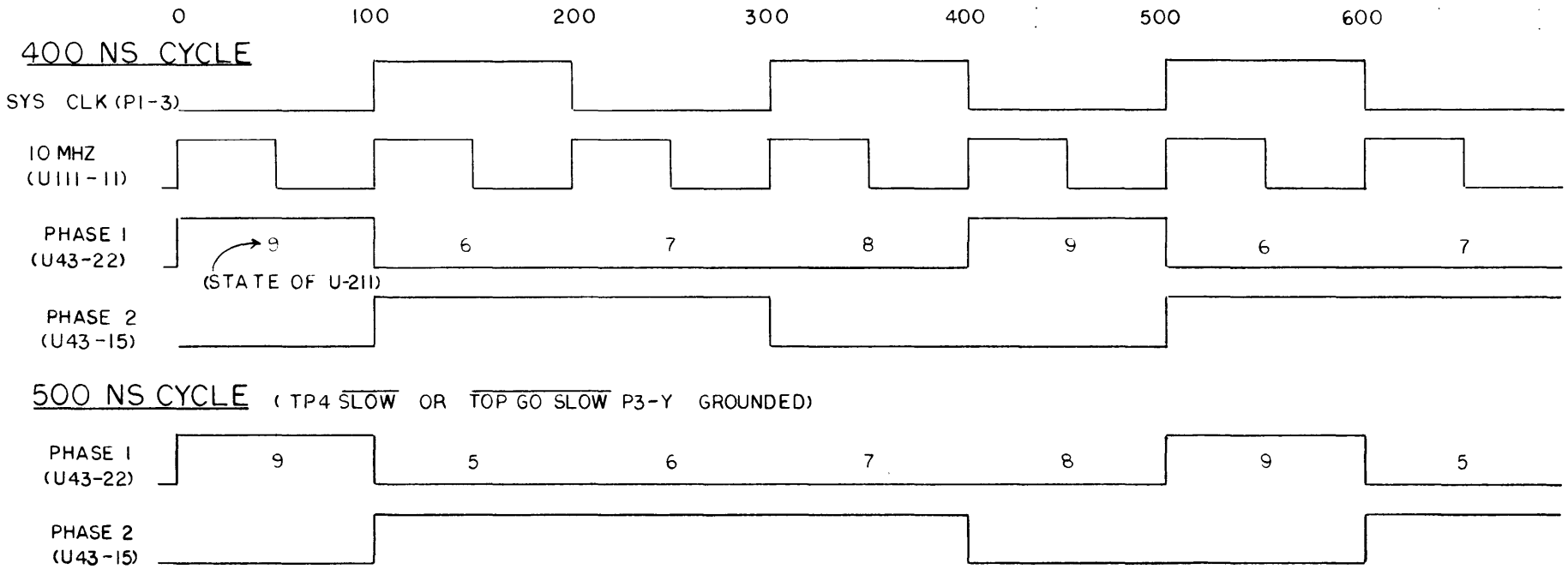

Figure 3
Clock Generator Timing Diagram
AUG-01-76 13255-91093

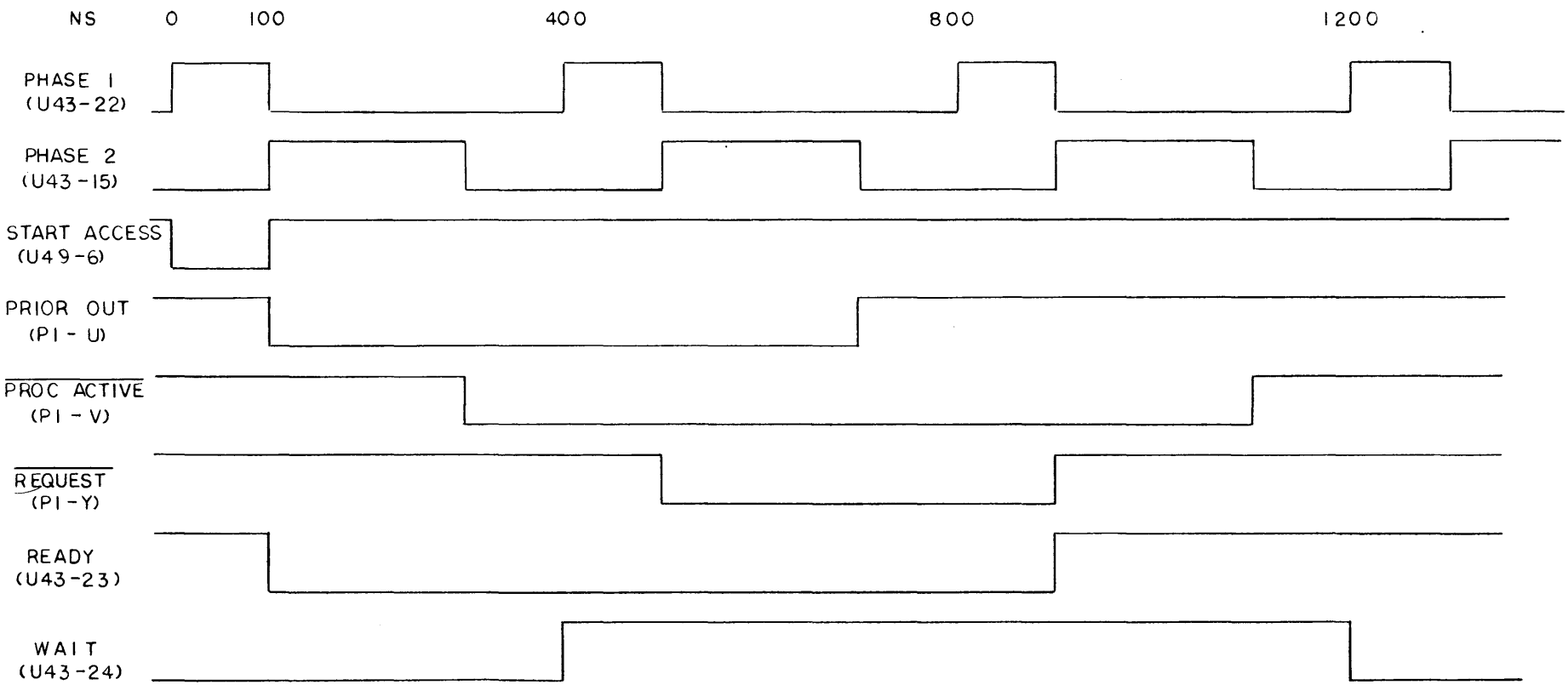

Figure 4
Bottom Bus Timing Diagram
AUG-01-76 13255-91093

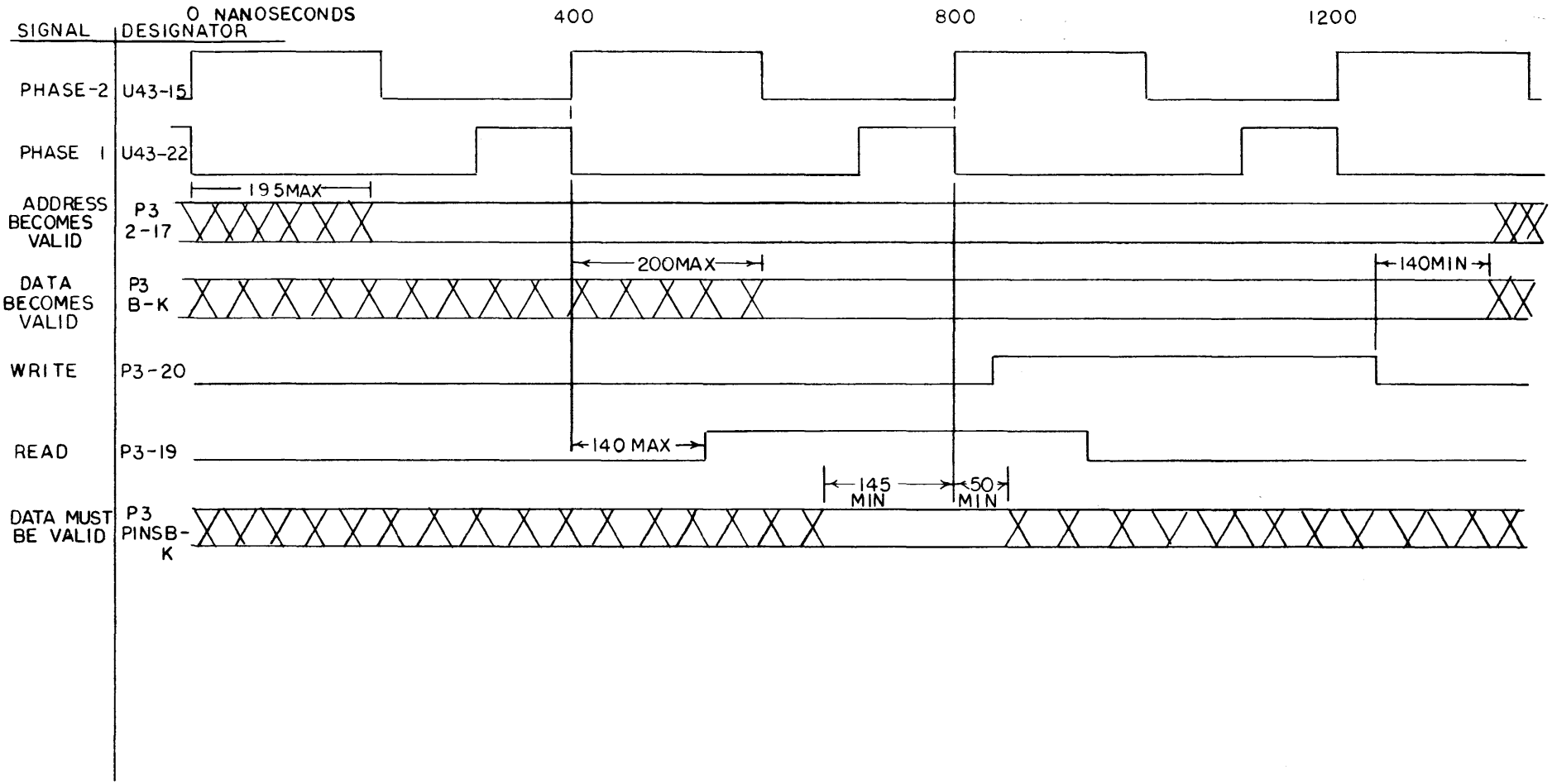

Figure 5
Top Bus Timing Diagram
AUG-01-76 13255-91093

Reference Designation	HP Part Number	Qty	Description	Mfr Code	Mfr Part Number
	02640-60093	1	PROCESSOR (8080A-2) ASSEMBLY DATE CODE: B-1641-42 REVISION DATE: 11-19-76	28480	02640-60093
C1	0160-0228	2	CAPACITOR-FXD 22UF+-10% 15VDC TA	56289	1500226X901582
C2	0160-0174	2	CAPACITOR-FXD .47UF +80-20% 25WVDC CER	28480	0160-0174
C4	0160-0228		CAPACITOR-FXD 22UF+-10% 15VDC TA	56289	1500226X901582
C5	0160-0174		CAPACITOR-FXD .47UF +80-20% 25WVDC CER	28480	0160-0174
C3	0160-0121		CAPACITOR-FXD 0.1UF	28480	0160-0121
C6	0160-0938	1	CAPACITOR- 1000PF 5%		0160-0938
C7	0160-2204	1	CAPACITOR-FXD 100PF +-5% 300WVDC MICA	28480	0160-2204
C8	0160-2055	9	CAPACITOR-FXD .01UF +80-20% 100WVDC CER	28480	0160-2055
C9	0160-2055		CAPACITOR-FXD .01UF +80-20% 100WVDC CER	28480	0160-2055
C10	0160-2055		CAPACITOR-FXD .01UF +80-20% 100WVDC CER	28480	0160-2055
C11	0160-2055		CAPACITOR-FXD .01UF +80-20% 100WVDC CER	28480	0160-2055
C12	0160-2055		CAPACITOR-FXD .01UF +80-20% 100WVDC CER	28480	0160-2055
C13	0160-2055		CAPACITOR-FXD .01UF +80-20% 100WVDC CER	28480	0160-2055
C14	0160-2055		CAPACITOR-FXD .01UF +80-20% 100WVDC CER	28480	0160-2055
C15	0160-2055		CAPACITOR-FXD .01UF +80-20% 100WVDC CER	28480	0160-2055
C16	0160-2055		CAPACITOR-FXD .01UF +80-20% 100WVDC CER	28480	0160-2055
CR1	1902-3090	1	DIODE-ZNR 4.99V 10% DO-7 PD=.4W	04713	SZ 10939-94
E1	0360-0124	6	TERMINAL-STUD SGL-PIN PRESS-MTG	28480	0360-0124
E2	0360-0124		TERMINAL-STUD SGL-PIN PRESS-MTG	28480	0360-0124
E3	0360-0124		TERMINAL-STUD SGL-PIN PRESS-MTG	28480	0360-0124
E4	0360-0124		TERMINAL-STUD SGL-PIN PRESS-MTG	28480	0360-0124
E5	0360-0124		TERMINAL-STUD SGL-PIN PRESS-MTG	28480	0360-0124
E6	0360-0124		TERMINAL-STUD SGL-PIN PRESS-MTG	28480	0360-0124
L1	9140-0114	1	COIL-MLD 10UH 10% Q=55 .155DX.375LG	99800	1537-36
R1	1810-0125	2	NETWORK-RES 8-PIN-SIP .125-PIN-SPCG	11236	750
R2	1810-0132	1	NETWORK-RES 8 X 500		
R3	1810-0125		NETWORK-RES 8-PIN-SIP .125-PIN-SPCG	11236	750
R4	0683-1025	3	RESISTOR 1K 5% .25W FC TC=-400/+600	01121	CB1025
R5	0683-1025		RESISTOR 1K 5% .25W FC TC=-400/+600	01121	CB1025
R9	0683-1015	2	RESISTOR 100 5% .25		
R6	0683-1025		RESISTOR 1K 5% .25W FC TC=-400/+600	01121	CB1025
R7	0683-4725	2	RESISTOR 4.7K 5% .25W FC TC=-400/+700	01121	CB4725
R8	0683-4725		RESISTOR 4.7K 5% .25W FC TC=-400/+700	01121	CB4725
R10	0683-1015	2	RESISTOR 100 5% .25		
U11	1820-1461	3	IC-DIGITAL SN74273N TTL OCTL D-TYPE	01295	SN74273N
U12	1820-1209	10	IC-DIGITAL SN74LS38N TTL LS QUAD 2 NAND	01295	SN74LS38N
U18	1820-1464	2	IC-DIGITAL SN74393N TTL DUAL BIN	01295	SN74393N
U19	1820-1464		IC-DIGITAL SN74393N TTL DUAL BIN	01295	SN74393N
U21	1820-1199	2	IC-DIGITAL SN74LS04N TTL LS HEX1	01295	SN74LS04N
U22	1820-1209		IC-DIGITAL SN74LS38N TTL LS QUAD 2 NAND	01295	SN74LS38N
U23	1820-1209		IC-DIGITAL SN74LS38N TTL LS QUAD 2 NAND	01295	SN74LS38N
U24	1820-1209		IC-DIGITAL SN74LS38N TTL LS QUAD 2 NAND	01295	SN74LS38N
U25	1820-1461		IC-DIGITAL SN74273N TTL OCTL D-TYPE	01295	SN74273
U26	1820-1461		IC-DIGITAL SN74273N TTL OCTL D-TYPE	01295	SN74273
U27	1820-1209		IC-DIGITAL SN74LS38N TTL LS QUAD 2 NAND	01295	SN74LS38N
U28	1820-1199		IC-DIGITAL SN74LS04N TTL LS HEX 1	01295	SN74LS04N
U29	1820-1112	1	IC-DIGITAL SN74LS74N TTL LS DUAL	01295	SN74LS74N
U31	1820-1758	1	IC		
U43	1820-1701	1	IC-DIGITAL C8080A-2 NMOS	34649	C8080A-2
U34	1820-1201	4	IC-DIGITAL SN74LS08N TTL LS QUAD 2 AND	01295	SN74LS08N
U35	1820-1197	1	IC-DIGITAL SN74LS00N TTL LS QUAD 2 NAND	01295	SN74LS00N
U36	1820-1144	2	IC-DIGITAL SN74LS02N TTL LS QUAD 2 NOR	01295	SN74LS02N
U37	1820-1201		IC-DIGITAL SN74LS08N TTL LS QUAD 2 AND	01295	SN74LS08N
U38	1820-1201		IC-DIGITAL SN74LS08N TTL LS QUAD 2 AND	01295	SN74LS08N
U51	1820-0987	1	IC-DIGITAL 93L18PC TTL L 8	07263	93L18PC
U41	1820-1049	2	IC-DIGITAL DM8097N TTL HEX 1 NON-INV	27014	DM8097N
U44	1820-1049		IC-DIGITAL DM8097N TTL HEX 1 NON-INV	27014	DM8097N
U45	1820-1209		IC-DIGITAL SN74LS38N TTL LS QUAD 2 NAND	01295	SN74LS38N
U41	1820-1470	1	IC-SN74LS157N		SN74LS157N
U46	1820-1209		IC-DIGITAL SN74LS38N TTL LS QUAD 2 NAND	01295	SN74LS38N
U47	1820-1144		IC-DIGITAL SN74LS02N TTL LS QUAD 2 NOR	01295	SN74LS02N
U48	1820-1203	1	IC-DIGITAL SN74LS11N TTL LS TPL 3 AND	01295	SN74LS11N
U49	1820-0054	1	IC-DIGITAL SN7400N TTL QUAD 2 NAND	01295	SN7400N
			IC-DIGITAL SN74LS00N TTL LS QUAD 2 NAND	01295	SN74LS00N
		1			
U58	1820-1209		IC-DIGITAL SN74LS38N TTL LS QUAD 2 NAND	01295	SN74LS38N
U59	1820-1202	1	IC-DIGITAL SN74LS10N TTL LS TPL 3 NAND	01295	SN74LS10N
U61	1820-1209		IC-DIGITAL SN74LS38N TTL LS QUAD 2 NAND	01295	SN74LS38N
U62	1820-1209		IC-DIGITAL SN74LS38N TTL LS QUAD 2 NAND	01295	SN74LS38N

Reference Designation	HP Part Number	Qty	Description	Mfr Code	Mfr Part Number
			PROCESSOR (8080A-2) ASSEMBLY CONT'D.		
U110	1820-1213	3	IC-DIGITAL SN74LS113N TTL LS DUAL	01295	SN74LS113N
U111	1820-1211	1	IC-DIGITAL SN74LS86N TTL LS QUAD 2	01295	SN74LS86N
U210	1820-1208	1	IC-DIGITAL SN74LS32N TTL LS QUAD 2 OR	01295	SN74LS32N
U211	1820-1429	1	IC-DIGITAL SN74LS160N TTL LS DECD	01295	SN74LS160N
U310	1820-1411	2	IC-DIGITAL SN74LS75N TTL LS D-TYPE	01295	SN74LS75N
U311	1820-1411		IC-DIGITAL SN74LS75N TTL LS D-TYPE	01295	SN74LS75N
U410	1820-1213		IC-DIGITAL SN74LS113N TTL LS DUAL	01295	SN74LS113N
U411	1820-0683	1	IC-DIGITAL SN74S04N TTL S HEX 1	01295	SN74S04N
U510	1820-1213		IC-DIGITAL SN74LS113N TTL LS DUAL	01295	SN74LS113N
U511	1820-1201		IC-DIGITAL SN74LS08N TTL LS QUAD 2 AND	01295	SN74LS08N
W1	1200-0483	1	SOCKET-IC 14-CONT DIP-SLDR	91506	514-AG11D
	1258-0124	6	PIN-PROGRAMMING JUMPER;.30 CONTACT	91506	8136-475G1
U32	1820-1828	2	IC-DIGITAL SIG 8T28		
U33	1820-1828		IC-DIGITAL SIG 8T28		
	1200-0552	1	SKT 40 DIP LO DS		